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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/246,303	02/08/99	LIN M	MSLIN98-005

TM02/0323

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EXAMINER	
PEYTON, T	
ART UNIT	**PAPER NUMBER**
2182	3

DATE MAILED: 03/23/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/246,303	LIN
Examiner	**Group Art Unit**
Tammara Peyton	2182

☒ Responsive to communication(s) filed on *Feb 8, 1999*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-51* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-51* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). *2*

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

1. Claims 1-51 are pending for application 09/246,303 filed on 02/08/99.

Specification

2. In the specification, page 5, line 15, reference to Figure 2, step "220" should be changed to "215". Correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Applicant Admission of Prior Art, (hereafter AAPA)* and *Chia et al., (hereafter Chia)*, patent number 6,054,767.

5. As per claims 1- 4, 10-12, 15, and 19-26, *AAPA* teaches that a DRAM or a computational processor chip type are a known good integrated circuit die having multiple selectable functions, multiple selectable output functions selecting logic states, common functions, a function selector, and all interconnected and connected to memory, data, timing, and address transfer input/output pads.

6. *Chia* teaches a method of an integrated circuit (IC) module (100, Fig.1) having a integrated circuit die (115, Fig.1) having selectable functions that is connected to input/output pads. *Chia* also teaches of a programmable substrate which the IC die is mounted having connections to the input/output pads to selectively connect the traces of the IC die to vias corresponding to desired pins, balls, or columns of the IC enabling transfer signals thereby producing an IC package that provides physical and electrical connections between the inherent wiring connection on the programmable substrate and an external circuitry. [Note Abstract, Summary, col. 4, lines 1 -col. 6, lines 1-50]

7. The system taught by *Chia* is design for an assembly manufacturer having to service different customers with different IC die connections, without substituting different substrates for each of the different IC die. The selection of functions pins for the programmable substrate associated with each IC changes depending on the current customer. It would have been obvious to one of ordinary skill that the IC taught by *Chia* would have been an IC well known in the art,

as disclosed by *AAPA*, therefore, the IC would inherently have multiple selectable input/output functions and appropriate logic states functions interconnected and connected to the input/output pads to enable communication with an external circuitry.

8. As per claim 5, it is well known technique in the art of input/output pads being created during processing of a semiconductor wafer.

9. As per claims 6, 7, 27, 28, it is a well known technique in the art of IC being attached to a substrate by a flip chip assembly and wherein input/output pads are gang-bonded to a substrate.

10. As per claims 8, 16-18, 29, *Chia* teaches wherein the input/output pads have solder bump and are arranged as a ball grid array, therefore it would have been obvious that non-selected input/output pads are omitted from connection to the programmable substrate.

11. As per claims 9 and 30, it would have been obvious to one skill in the art that the programmable substrate taught by *Chia* could be selected from the group of substrates as claimed. [col. 4, lines 19-25]

12. As per claims 13 and 14, please see paragraphs respectfully 4-6.

13. As per claims 31, 38, and 45, *AAPA-Chia* teaches a system method of an integrated circuit (IC) module (100, Fig.1) having a integrated circuit die (115, Fig.1) having selectable functions that is connected to input/output pads wherein the IC die is arranged in rows and columns to form a Ball Grid Array therefore *AAPA-Chia* teaches the code to implement the method. [See paragraph 10]

14. As per claims 32-37, 39-44, 46-51, please see paragraphs 4-13.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (703) 306-5508. The examiner can normally be reached between 8:00 - 4:30 from Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee, can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3718.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

Faxes for formal communications intended for entry should be sent to:

(703) 308-9051,

or, for informal or draft communications, to:

(703) 306-5404 (please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to:

Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Tammara Peyton

March 20, 2001

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100